QBDTUMEG010241M

Cisco® Compatible TAA 400GBase-Open ZR+ Coherent QSFP-DD Transceiver (SMF, Tunable, 120km, LC, DOM, 4dBm)

Product Description

This Cisco® QSFP-DD transceiver provides 400GBase-Open ZR+ throughput up to 120km over single-mode fiber (SMF) using a tunable wavelength via an LC connector. It is guaranteed to be 100% compatible with the equivalent Cisco® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

Skylane's transceivers are RoHS compliant and lead-free.

Features:

- Hot Pluggable QSFP-DD Footprint (Type 2A)
- Duplex LC Connector
- Supports 400/300/200/100Gbps
- Coherent Receivers
- Power Dissipation is 22.5W
- Tunable C-Band Transmitter
- Operating Case Temperature: 15 to 75 Celsius
- Single +3.3V Power Supply
- Supports both CFEC and oFEC RoHS Compliant and Lead Free
- Tunable Power, max TX power +4dBm at 193.7THz +1dBm at C band

Applications:

- 400GBase Ethernet
- Open ZR+

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

Applications Supported

Description	Host Format	Modulation	FEC	Range (Note 1)	DAC-Rate	CD	
						Min	Max
OIF 400ZR app code 0x001	1 x 400GAUI-8	16QAM	CFEC	120km	1x1.50	-2400	2400
OpenZR+ MSA	1 x 400GAUI-8	16QAM	oFEC	450km	1x1.50	-26000	26000
Open ZR+ MSA	4 x 100GAUI-2	16QAM	oFEC	450km	1x1.25	-26000	26000
Open ZR+ MSA	4 x 100GAUI-2	16QAM	oFEC	450km	1x1.50	-26000	26000
Open ZR+ MSA	3 x 100GAUI-2	8QAM	oFEC	600km	1x1.50	-50000	50000
OpenZR+ MSA	2 x 100GAUI-2	QPSK	oFEC	1000km	1x1.50	-50000	50000
Open ZR+ Extension	2 x 100GAUI-2	8QAM	oFEC	2000km	1x1.25	-50000	50000
Open ZR+ Extension	2 x 100GAUI-2	16QAM	oFEC	2000km	1x1.25	-50000	50000
OpenZR+ MSA	1 x 100GAUI-2	QPSK	oFEC	2000km	1x1.50	-80000	80000

Note:

1. Amplified: -10dBm to +1dBm output power @ C-band.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Maximum Supply Voltage	Vcc	-0.3	3.3	3.6	V	Not damaged
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Storage Relative Humidity	RH	5		85	%	Non-condensing
Operating Relative Humidity	RH	15		85	%	
Receiver Damage Threshold	PRdmg	10			dBm	Total optical power
ESD Sensitivity				1000	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	TC	0		70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
	ICC			7.2	A	
Maximum Sustained Peak Current (<500ms)				7.4	A	
Maximum Instantaneous Peak Current (<50us)				9	A	
Electro-Static Discharge	ESD			1000	V	
Power Consumption	PD		22	22.5	W	1

Relative Humidity		RH	15		85	%	
Client Mode	**400G (400ZR)**		1 x 400GAUI-8				
			4 x 100GAUI-2				
	400G (400ZR+)		1 x 400GAUI-8				
			4 x 100GAUI-2				
	300G (300ZR+)		3 x 100GAUI-2				
	200G (200ZR+)		2 x 100GAUI-2				
			2 x CAUI-4				
	100G (100ZR+)		1 x 100GAUI-2				
			1 x CAUI-4				
Transmission Distance	**400G (400ZR)**				120	km	
	400G (400ZR+)				450	km	
	300G (300ZR+)				600	km	
	200G (200ZR+)				1000	km	
	100G (100ZR+)				2000	km	
Power Supply Noise		Vrip			1%	DC-1MHz	
		Vrip			2%	1-10MHz	

Notes:

1. In 400GbE mode, the typical power consumption is 22W and the maximum power consumption is 22.5W. When switching to 4×100GbE mode, the typical power consumption will be 23W and the maximum power consumption will be 23.5W, the current will also change accordingly.

High-Speed Electrical Characteristics 400GAUI-8 C2M and 100GAUI-2 C2M

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter					
Signaling Rate, Each Lane		26.5625 ± 100 ppm		GBd	PAM-4
AC Common-Mode Output Voltage (RMS)	RMS		17.5	mV	
Differential Voltage Pk-Pk	Vin, pp	750	900	mV	
Near-end ESMW (Eye Symmetry Mask Width)		0.265		UI	Non-condensing
Near-end Eye Height, Differential		70		mV	
Far-end ESMW		0.2		UI	Total optical power
Far-end Eye Height, Differential		30		mV	
Far-end Pre-Cursor ISI Ratio		-4.5	2.5	%	
Differential Output Return Loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 120E
Common to Differential Mode Conversion Return Loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	At 1 MHz

Transition Time (20% to 80%)	Trise/Tfall	9.5		Ps	20% to 80%
DC Common Mode Voltage	Vcm	-350	2850	mV	
Receiver					
Signaling Rate Per Lane		26.5625 ± 100 ppm		GBd	PAM-4
Differential Pk-Pk Input Voltage Tolerance	Vout, pp	900		mV	
Differential Input Return Loss (min)		Equation (83E–5)			IEEE Std 802.3-2018 Annex 120E
Differential to Common-Mode Input Return Loss (min)		Equation (83E–6)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	
Module Stressed Input Test		See 120E.3.4.1			IEEE Std 802.3-2018 Annex 120E
Single-Ended Voltage Tolerance Range (min)		-0.4	3.3	V	
DC common mode voltage(min)		-350	2850	mV	

High-Speed Electrical Characteristics CAUI-4 C2M

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter					
Signaling Rate, Each Lane		25.78125 ± 100 ppm		GBd	NRZ
AC Common-Mode Output Voltage (RMS)	RMS		17.5	mV	
Differential Voltage Pk-Pk	Vin, pp	750	900	mV	
Eye Width		0.57		UI	
Eye Height, Differential		228		mV	
Vertical Eye Closure		5.5		dB	
Differential Output Return Loss		Equation (83E-2)			IEEE Std 802.3-2018 Annex 120E
Common to Differential Mode Conversion Return Loss		Equation (83E-3)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	At 1 MHz
Transition Time (20% to 80%)	Trise/Tfall	9.5		Ps	20% to 80%
DC Common Mode Voltage	Vcm	-350	2850	mV	
Receiver					
Signaling Rate Per Lane		25.78125 ± 100 ppm		GBd	NRZ
Differential Pk-Pk Input Voltage Tolerance	Vout, pp	900		mV	
Differential Input Return Loss (min)		Equation (83E–5)			IEEE Std 802.3-2018 Annex 120E
Differential to Common-Mode Input Return Loss (min)		Equation (83E–6)			IEEE Std 802.3-2018 Annex 120E
Differential Termination Mismatch			10	%	

Module Stressed Input Test		See 83E.3.4.1			
Single-Ended Voltage Tolerance Range (min)		-0.4	3.3	V	
DC common mode voltage(min)		-350	2850	mV	

Low-Speed Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
SCL and SDA	VOL	0	0.4	V	1
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O Signal	Ci		14	pF	
Total Bus Capacitive Load for SCL and SDA	Cb		100	pF	2
	Cb		200	pF	3
InitMode, ResetL and ModSelL IntL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	10k ohms pull up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0mA
	VOH				4

Notes:

1. IOL(max)=3mA for fast mode, 20ma for Fast-mode plus.
2. For 400kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 45 (QSFP-DD-Hardware-rev5p0).
3. For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 45 (QSFP-DD-Hardware-rev5p0)
4. ModPrsL can be implemented as a short-circuit to GND on the module.

Optical Characteristics

Parameter		Min.	Typ.	Max.	Unit	Notes
Transmitter						
Modulation Format	**400G**	ZR400-CFEC-16QAM				CFEC FEC, NCG 10.8dB
		ZR400-OFEC-16QAM				OFEC FEC, NCG 11.6dB
	300G	ZR300-OFEC-8QAM				
	200G	ZR200-OFEC-QPSK				
	100G	ZR100-OFEC-QPSK				
Baud Rate	**400G**	59.843750000±20ppm			GBd	
		60.138546798±20ppm			GBd	
	300G	60.138546798±20ppm			GBd	
	200G	60.138546798±20ppm			GBd	
	100G	30.069273399±20ppm			GBd	
Transmitter Frequency Range		191.3		196.1	THz	
Flexible DWDM Grid		6.25			GHz	
Frequency Fine Tuning Range		-5		5	GHz	Bright tuning
Frequency Fine Tuning Step		0.1			GHz	
Laser Frequency Accuracy		-1.8		1.8	GHz	
TX Spectral Upper Mask				(30.0, 0.0) (37.0,-1 0.0) (39.2,-1 5.0) (40.4,-2 0.0)	(GHz,d B)	1
TX Spectral Lower Mask		(30.0,-9.0) (31.3,-2 0.0) (31.3,-3 5.0)			(GHz,d B)	2
Transmitter Laser Disable Time				100	ms	
Transmitter Wavelength Switching Time				60	s	
Transmitter Laser Enable Time				10	s	
Transmit Output Power Adjustable Range		-10		1	dBm	3
Transmit Output Power Adjust Step		0.1			dB	
Optical Power Setting Accuracy		-1		1	dB	4
Output Power Monitor Accuracy		-1		1	dB	
Power Stability		-0.5		0.5	dB	At fixed wavelength, room temperature
		-1		1	dB	5
Total Output Power with Tx Disabled				-20	dBm	
Total Output Power During Wavelength Switching				-20	dBm	
Transmitter Reflectance				-20	dB	Looking into the Tx

Inband (IB) OSNR		38			dB		
Lorentzian Linewidth				300	kHz	Tx and LO	
Relative Intensity Noise				-140	dB/Hz		
Mean I-Q Amplitude Imbalance				1	dB		
Transmitter Polarization Dependent Power				1.5	dB		
DC I-Q Offset (Mean per Polarization)				-26	dB		
I-Q Instantaneous Offset				-20	dB		
Receiver							
Modulation Format	**400G**	ZR400-CFEC-16QAM				CFEC FEC, NCG 10.8dB	
	400G	ZR400-OFEC-16QAM				OFEC FEC, Net Coding Gain(NCG) 11.6dB，Thretical Max PreFEC BER 2.0E-2	
	300G	ZR300-OFEC-8QAM					
	200G	ZR200-OFEC-QPSK					
	100G	ZR100-OFEC-QPSK					
Baud Rate	**400G**	59.843750000±20ppm			GBd	400ZR,SFF-8024 Media ID 3Eh/3Fh	
	400G	60.138546798±20ppm			GBd	400ZR+, SFF-8024 Media ID 46h	
	300G	60.138546798±20ppm			GBd	300ZR+, SFF-8024 Media ID 47h	
	200G	60.138546798±20ppm			GBd	200ZR+, SFF-8024 Media ID 48h	
	100G	30.069273399±20ppm			GBd	100ZR+, SFF-8024 Media ID 49h	
Frequency Offset Between Received Carrier and LO		-3.6		+3.6	GHz		
Input Power Range	**400G**	-12		0	dBm	Signal power, OSNR>26dB,400ZR	
	400G	-12		0	dBm	Signal power, OSNR>24dB,400ZR+	
	300G	-15		0	dBm	Signal power, OSNR>21dB,300ZR+	
	200G	-18		0	dBm	Signal power, OSNR>16dB,200ZR+	
	100G	-18		0	dBm	Signal power, OSNR>12.5dB,100ZR+	
OSNR Tolerance	**400G**			26	dB/0.1nm	400ZR	Measured back-to-back with short optical channel
	400G			24	dB/0.1nm	400ZR+	
	300G			21	dB/0.1nm	300ZR+	
	200G			16	dB/0.1nm	200ZR+	
	100G			12.5	dB/0.1nm	100ZR+	
RX Sensitivity	**400G**	-20			dBm	400ZR	Inband (IB) OSNR ≥34dB
Non-damaging Input Power				10	dBm	Total power	
Optical Input Power Monitor Accuracy		-2		2	dB	Total power	
MAX FEC Pre Ber		0.017		0.020			

Chromatic Dispersion Tolerance	**400G**			2,400	ps/nm	400ZR	Tolerance to CD with ≤0.5 dB penalty to OSNR sensitivity when change in SOP is ≤1 rad/ms
				20,000	ps/nm	400ZR+	
	300G			40,000	ps/nm	300ZR+	
	200G			50,000	ps/nm	200ZR+	
	100G			100,000	ps/nm	100ZR+	
CD Monitor Accuracy		-200		200	ps/nm		
DGD Tolerance	**400G**	33			ps	400ZR	OSNR penalty<0.5dB
		66			ps	400ZR+	
	300G	83			ps	300ZR+	
	200G	83			ps	200ZR+	
	100G	100			ps	100ZR+	
DGD Monitor Accuracy		-15		15	ps	6	
Peak PDL Tolerance				3.0	dB	7	
				3.5	dB	8	
Tolerance to Change in SOP		50			krad/s	9	
Optical Return Loss		20			dB	Optical reflectance at Rx connector input.	
Optical Rx_LOS Assert Threshold	**400G**	-20	-18	-16	dBm		
	300G	-23	-21	-19	dBm		
	200G	-26	-24	-22	dBm		
	100G	-26	-24	-22	dBm		
Optical Rx_LOS Hysteresis		1	1.5	2.5	dB		
Optical Input Power Transient Tolerance		-2		2	dB		
Service Recovery Time				40	ms		

Notes:

1. Refer to OIF-400ZR-02.0 13.3.201b.
   Refer to openzrplus_2p0 11.4.10.
2. Refer to OIF-400ZR-02.0 13.3.201b.
   Refer to openzrplus_2p0 11.4.10.
3. The absolute accuracy is ±1dB.
4. Difference between setting and reporting.
5. At fixed wavelength, environment temperature.
6. 0~40ps for 400ZR
   0~100ps for 400/300/200/100ZR+
7. Tolerance to peak PDL with ≤1.3dB additional OSNR penalty when change in SOP is ≤1 rad/ms.
8. Tolerance to peak PDL with ≤1.8dB additional OSNR penalty when change in SOP is ≤1 rad/ms.
9. With ≤ 0.5 dB additional OSNR penalty over all PMD and PDL values.
10. Tolerance to change in input power with < 0.5 dB penalty to OSNR tolerance.
    The 20% to 80% rise/fall times for the input power change shall be no faster than 50 μs.

11. The transmitter and receiver comply with the 400GAUI-8 C2M and CEI-56G-VSR-PAM4 electrical specification, Electrical interface definitions see IEEE Std 802.3-2018 Annex 120E. The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInitDuration	Max MgmtInit		2000	ms	1
ResetL Assert Time	t_reset_init	10		us	2
IntL Assert Time	ton_IntL		200	ms	3
IntL De-assert Time	toff_IntL		500	us	4
Rx LOS Assert Time	ton_los		100	ms	5
Rx LOS Assert Time (Optional Fast Mode)	ton_losf		10	ms	6
Rx LOS De-assert Time	toff_los		100	ms	
Tx Fault Assert Time	ton_Txfault		200	ms	7
Flag Assert Time	ton_flag		200	ms	8
Mask Assert Time	ton_mask		100	ms	9
Mask De-assert Time	toff_mask		100	ms	10
High Power Up State			180	s	
Software TX Disable Assert Time			100	ms	
Software TX Disable De-assert Time			10	s	

Notes:

1. Time from power on, hot plug or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx LOS, Tx Fault and other flag bits.
5. Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
6. Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
7. Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
8. Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
9. Time from mask bit set (value=1b) until associated IntL assertion is inhibited.
10. Time from mask bit cleared (value=0b) until associated IntL operation resumes.

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1

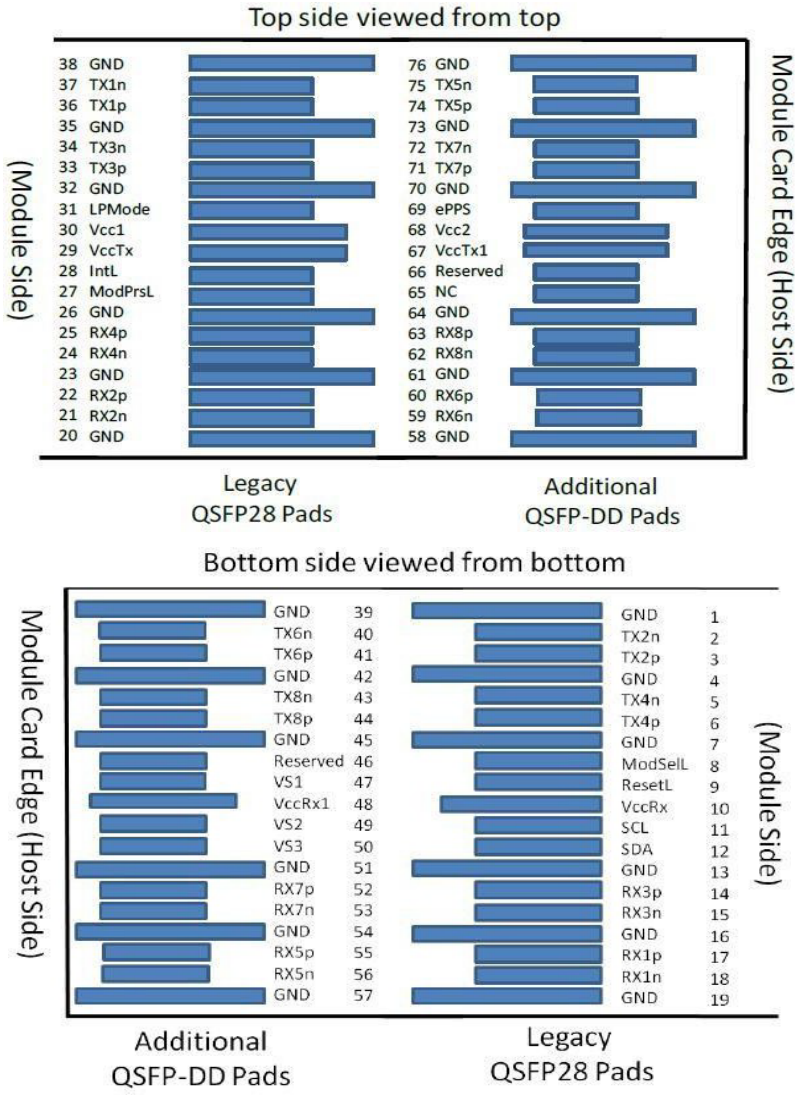
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input. Not used	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	

73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

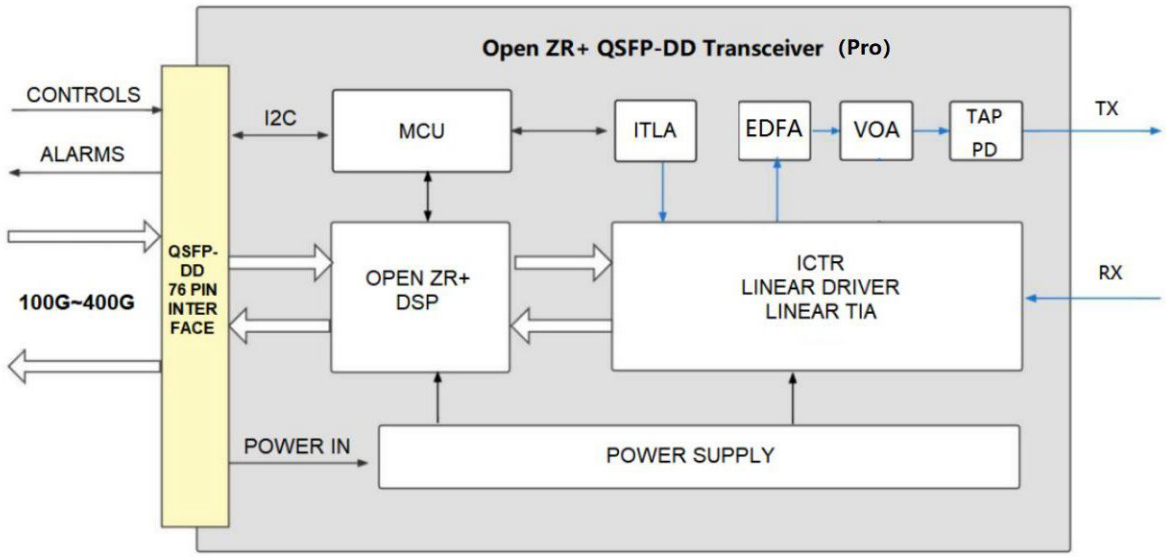
Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1500 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

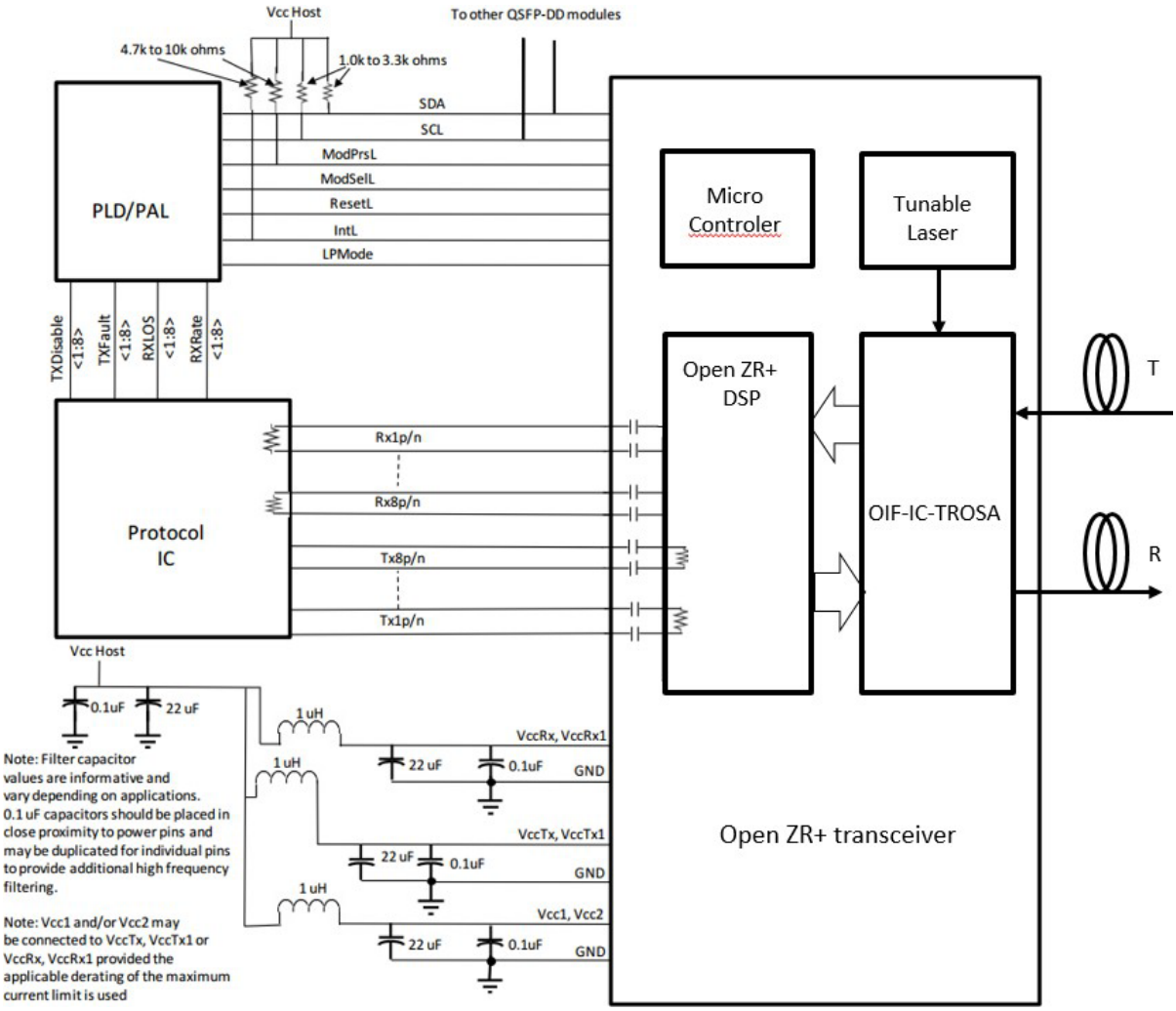
Electrical Pad Layout



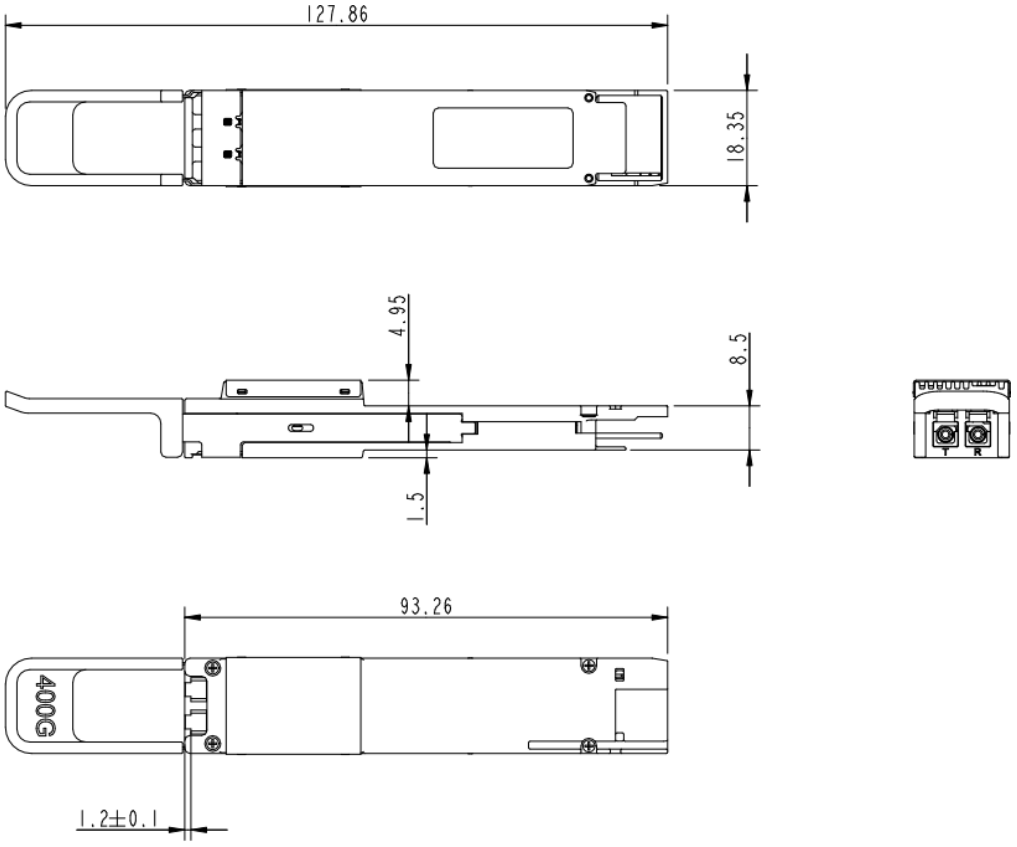
Block Diagram



Recommended Interface Circuit



Mechanical Specifications



About Skylane Optics

Skylane is a leading provider of transceivers for optical communication.

We offer an extensive portfolio for the enterprise, access, datacenter and metropolitan fiber optical market as well as for smart home applications and home networks.

We cover the European, South American and North American market with a strong partner network and have offices in Belgium, Brazil, Sweden and USA.

Our offerings are characterized by high quality and performance. In combination with our strong technical support, we enable our customers to build cost optimized network solutions.

We offer an extensive range of high-quality products including transceivers (Optical and copper), Active Optical Cable (AOC), Direct Attach Cable (DAC), Mux/Demux, Coding Box (SKYGATE).